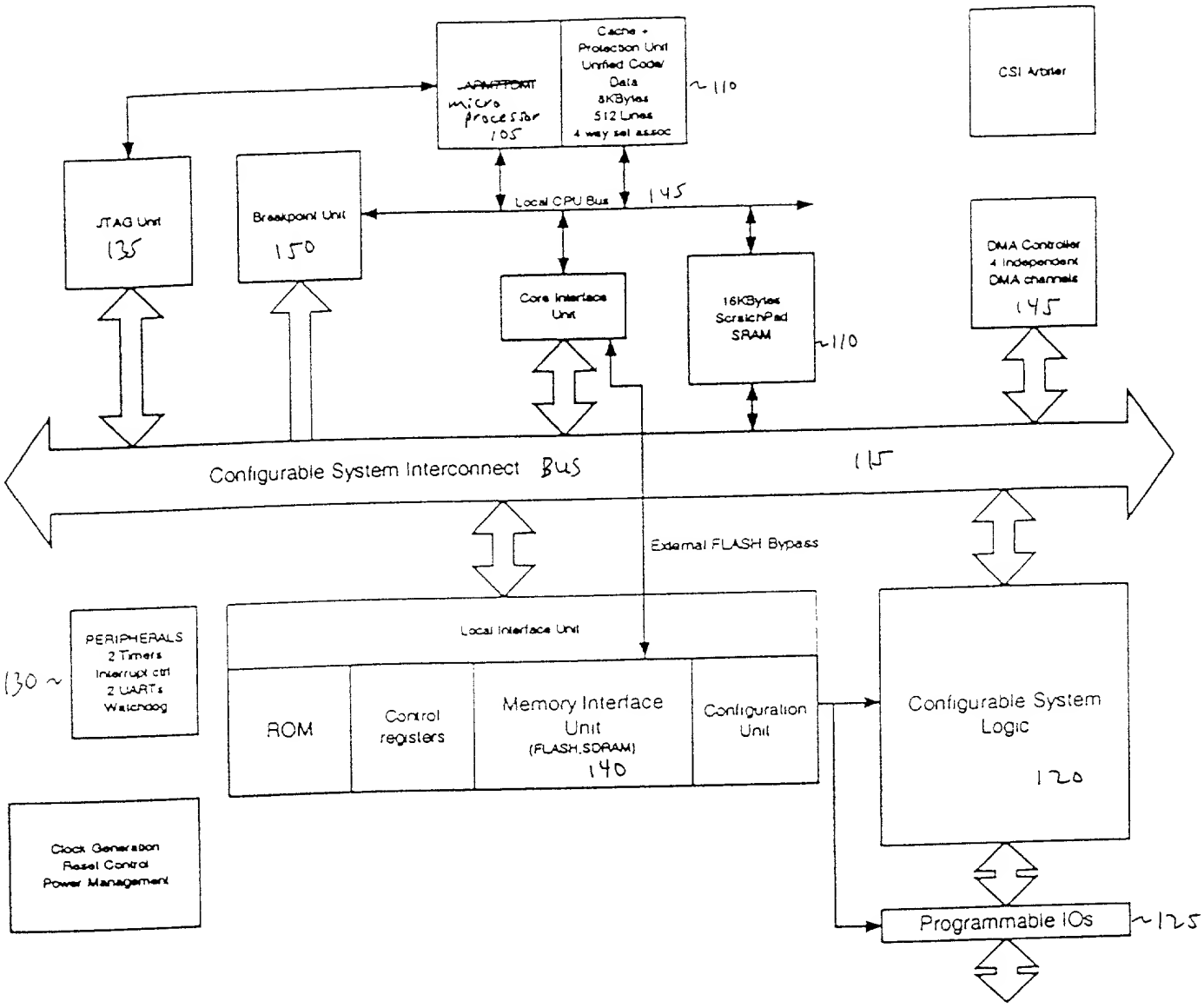

Cache + Protection Unit Unified Code/ Data 8KBytes 512 Lines 4 way set assoc
~110
micro processor 105
CSI Arbiter
JTAG Unit 135
Breakpoint Unit 150
Local CPU Bus
145
Core Interface Unit
16KBytes ScratchPad SRAM
~110
DMA Controller 4 independent DMA channels 145
Configurable System Interconnect Bus
115
External FLASH Bypass
Local Interface Unit
PERIPHERALS 2 Timers Interrupt ctrl 2 UARTs Watchdog
130 ~
ROM
Control registers
Memory Interface Unit (FLASH,SDRAM) 140
Configuration Unit
Configurable System Logic 120
Clock Generation Reset Control Power Management
Programmable IOs
~125

Figure 1

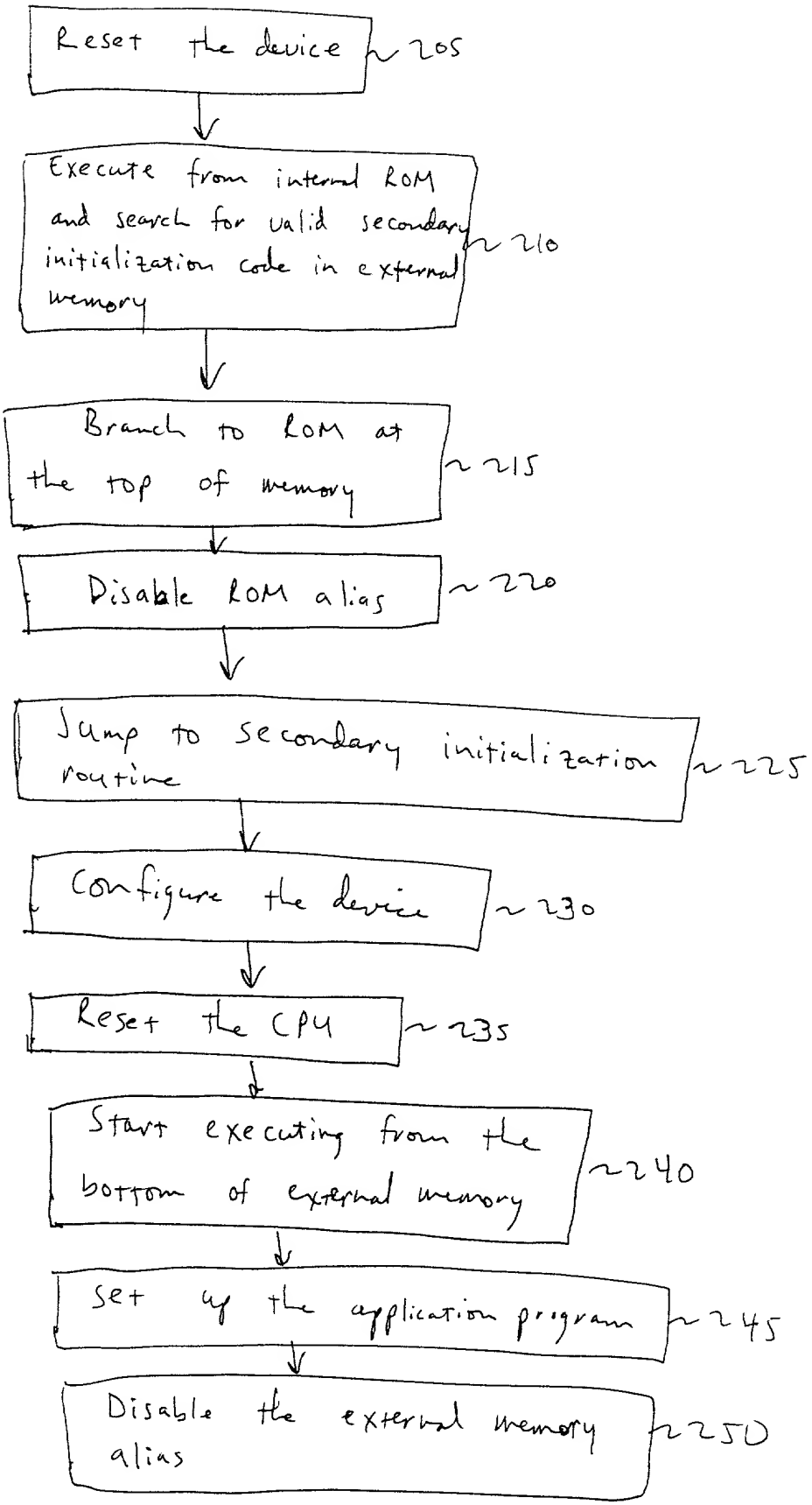
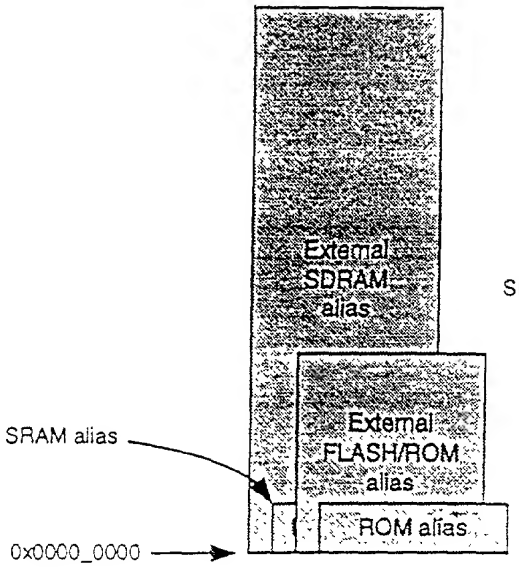
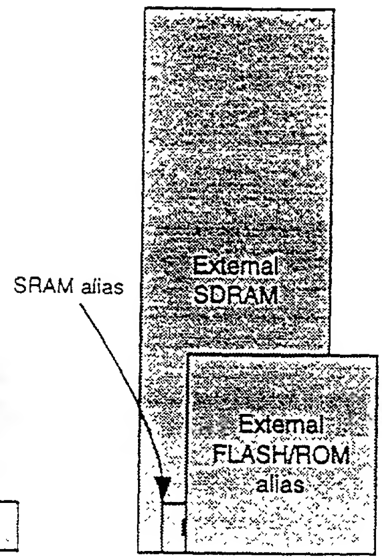

Reset the device
205
Execute from internal ROM and search for valid secondary initialization code in external memory
210
Branch to ROM at the top of memory
215
Disable ROM alias
220
Jump to secondary initialization routine
225
Configure the device
230
Reset the CPU
235
Start executing from the bottom of external memory
240
Set up the application program
245
Disable the external memory alias
250

Figure 2



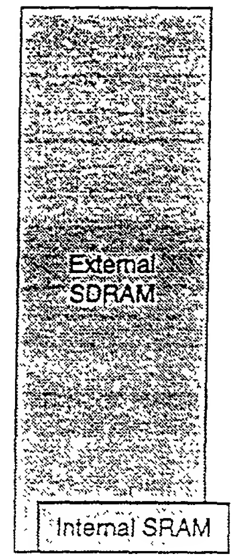
Device Configuration Phase

Figure 3A



Secondary Configuration and Start of Application

Figure 3B



Normal Operation Mode

Figure 3C